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MODELING THE SUBTHRESHOLD REGION DRAIN CURRENT FOR SYMMETRICAL DOUBLE-GATE JUNCTIONLESS MOSFETs

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ABSTRACT

A 1-Dimensional analytical solution for Poisson's equation is derived by using the surface potential based charge model for a symmetric double gate junctionless MOSFET by considering only the mobile charge carriers. On the basis of surface potential based charge model a relation between the surface potential and gate voltage is obtained in terms of Lambert-W function. Then the Pao-Sah integral is evaluated to obtain the drain current in the subthreshold region. The result of the obtained drain current model is being compared with the drain current of a symmetric double gate (DG) MOSFET in the subthreshold region. The model is then compared with the results of the Cogenda's Visual TCAD simulation tool and the model is being found to be in good agreement with the simulation results.

Keywords: *Junctionless, Double Gate, Simulation, Doping, Surface Potential, Drain Current*.

Introduction

With continuous device miniaturization, the device dimension has been scaled down to nanometer range which has increased the short channel effects (SCEs) considerably. To reduce these SCEs and increase the current capacity many multi-gate structures have been proposed [1-3]. Double gate (DG) MOSFETs proved to be pioneer in the field of nanoscale device dimensions but with continuous miniaturization the control of doping profile between the source/drain and channel region to suppress the SCEs is becoming challenging. To curve out this difficulty a novel structure is being proposed named double gate junctionless (JL) MOSFET [4] which has same doping profile throughout its structure that is either

n-n-n type or p-p-p type instead of conventional n-p-

n or p-n-p type MOSFETs. In junctionless MOSFET the bulk current conduction mechanism reduces the impact of imperfect insulator/semiconductor interfaces [5]. For an n-n-n type junctionless MOSFET the gate electric field pops the electron out of the body region for a lower gate bias voltage and thereby switching the transistor off by fully depleting the body region. Increase in gate voltage increases the electron concentration in the body region thereby eliminating the depletion region and at a point this increasing electron concentration equalizes with the body doping concentration N_{si} and makes the channel under the gate electrically neutral. The junctionless MOSFET being an accumulation mode majority carrier device with further increase in gate voltage increases the electron accumulation in the channel beneath the gate oxide which reduces the channel resistance and contributes to the current conduction between the source and drain region by turning the device on.

With the beneficial features of the DG JL MOSFET, compact analytical models are required to study the characteristics of the device. A number of drain current models have been proposed [6-7].Then a non piece wise model for DG JL MOSFET was developed using the parabolic potential approximation in the subthreshold region [8]. In this paper the Pao-Sah integral [9] is evaluated to obtain the subthreshold region drain current in terms of Lambert-W function by solving the Poisson's and current continuity equations using surface potential based charge model. The subthreshold drain current equation is modeled for a short channel double gate JL MOSFET by incorporating channel length modulation and DIBL (drain induced barrier lowering) parameter. The characteristics of the proposed

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model is compared with the subthreshold region drain current model for a symmetric DG MOSFET and a published drain current model for DG JL MOSFE and the proposed model is found to be in close agreement with both the models. The proposed model is validated using the TCAD simulation results.

Poisson's Equation

- **DG JL MOSFET**

In order to obtain the surface potential of the DG JL MOSFET the potential distribution in the silicon film of the device is studied. Figure 1 represents a schematic diagram of a DG JL MOSFET where the channel length is represented by L, t_{ox} and t_{si} represents the oxide thickness and silicon film thickness. N_{si} is the doping concentration in the channel and source/drain region.

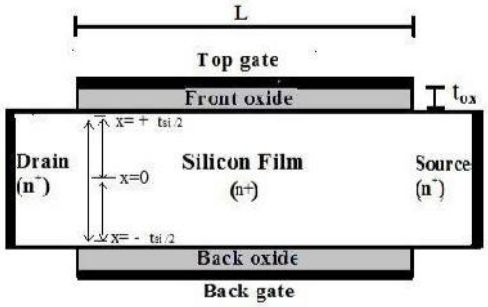


Fig. 1 Cross-section of DG JL MOSFET

Considering only the mobile charges, according to the classical model, the Poisson's equation in the channel region of Fig. 1 is given by:-

$$\frac{d^2\Psi_{jl}}{dx^2} = \frac{qN_{si}}{\varepsilon_{si}}\left[\exp\left(\frac{\Psi - V}{v_{thermal}}\right) - 1\right] \qquad \ldots (1)$$

where $\Psi_{a}(\xi)$ is the electrostatic channel potential,

$_{si}$ is the silicon permittivity, $v_{thermal}$ is the thermal voltage whose value is given by (KT/q) ≈ 26mV, V is the quasi-Fermi potential of the electron and q is the electronic charge.

DG JL MOSFET being a majority carrier device, the hole concentration is considered to be negligible compared to that of electrons in the channel with the boundary condition to be considered as:

$$\left.\frac{d\Psi_{jl}}{dx}\right|_{x=0} = 0 \qquad \ldots (2)$$

The electric potential a $\pm t_{si}/2$ is given by Ψ_{jls}

termed as surface potential and the potential at the centre of the film at x=0 is denoted by Ψ_{a0}.

Integrating (1) from $_{jl0}$ to $_{jls}$ once give:

$$\frac{d\Psi_{jl}}{dx} = \frac{2qN_{si}v_{thermal}}{\varepsilon_{si}}\left[\left(\exp\left(\frac{\Psi_{jls} - V}{v_{thermal}}\right) - \exp\left(\frac{\Psi_{jl0} - V}{v_{thermal}}\right)\right) + \left(\frac{\Psi_{jls} - \Psi_{jl0}}{v_{thermal}}\right)\right]$$

… (3)

Now using Gauss's law, the relation between the surface potential and the gate voltage can be obtained work function difference).

$$Q_O = 2\pounds_{si} \left.\frac{d\Psi_{jl}}{dx}\right|_{x=\pm t_{si}/2} \quad \ldots (4)$$

The space charge density within limits (Ψ_{jl0} to Ψ_{jls}) is given by:

$$Q_o = -2\pounds_{si} \frac{d\Psi_{jl}}{dx} = -2C_{ox}\left(\Psi_g - \Psi_{fb} - \Psi_{jls}\right) \quad \ldots (5)$$

Where C_{ox} is oxide capacitance, Ψ_g is the gate voltage, Ψ_{fb} is the flat band voltage ($\Psi_{fb} \approx \Phi_{MS}$, the

The channel potential by using parabolic potential approximation [10] is designated by:

$$\Psi_{jl}(x) = \left(\frac{4x^2}{t_{si}^2}\right)\left(\Psi_{jls} - \Psi_{jl0}\right) + \Psi_{jl0} \quad \ldots (6)$$

Differentiating (6) with respect to x we get

$$\frac{d\Psi_{jl}}{dx} = \frac{4(2x)}{t_{si}^2}(-\Delta\Psi_{jl}) \quad \ldots (7)$$

where $\Delta\Psi_{jl} = \Psi_{jl0} - \Psi_{jls}$

Using (5) and (7) we obtain

$$\frac{C_{ox}}{\pounds_{si}}(\Psi_g - \Psi_{fb} - \Psi_{jls}) = -\frac{4(2x)}{t_{si}^2}(\Delta\Psi_{jl}) \quad \ldots (8)$$

As he channel is considered to be fully depleted Ψ_{jl0} is approximately zero.

$$\frac{C_{ox}}{\pounds_{si}}(\Psi_g - \Psi_{fb} + \Delta\Psi_{jl}) = -\frac{4\Delta\Psi_{jl}}{t_{si}} \quad \ldots (9)$$

$\Delta\Psi_{jl}$ of (9) is equivalent to [11]

$$\Delta\Psi_{jl} = \frac{t_{si}}{8\pounds_{si}}\left(Q_{mobile} + qN_{si}t_{si}\right) \quad \ldots (10)$$

Putting (10) in (9) and solving by assuming Q_{mobile} to be zero, the threshold voltage can be directly obtained at gate voltage, $\Psi_g = V_{th}$ as:

$$V_{th} = \Psi_{fb} - \frac{qN_{si}t_{si}^2}{8\pounds_{si}} - \frac{qN_{si}t_{si}}{2C_{ox}} \quad \ldots (11)$$

Solving (3) and (5) we obtain,

$$(\Psi_g - \Psi_{fb} - \Psi_{jls}) = \sqrt{\frac{2qN_{si}\varepsilon_{si}V_{thermal}}{C_{ox}}\left\{1-\exp\left[\left(\frac{\Psi_{jl0}-V}{V_{thermal}}\right)\left(\frac{1-\exp(-\varepsilon)}{\varepsilon}\right)\right]\right\}} \quad \ldots (12)$$

where $\varepsilon = -\left(\frac{\Psi_{jls}-\Psi_{jl0}}{V_{thermal}}\right)$, for subthreshold region the term inside the square root $\left(\frac{1-\exp(-\varepsilon)}{\varepsilon}\right) << 1$,

thereby modifying the above equation as:-

$$(\Psi_g - \Psi_{fb} - \Psi_{jls}) = -\frac{qN_{si}t_{si}}{2C_{ox}}\left[1+\frac{1}{2}\left(\frac{V-\Psi_{jl0}}{V_{thermal}}\right)\right] \quad \ldots (13)$$

Finally the relation between the surface potential and gate voltage for DG JL MOSFET in terms of Lambert-W function is explicitly obtained as:

$$\Psi_{jls} = \Psi_g - V_{th} - \frac{qN_{si}t_{si}^2}{8\varepsilon_{si}} - V_{thermal}W[A] \quad \ldots (14)$$

where $A = \frac{N_{si}qt_{si}}{4V_{thermal}C_{ox}}\exp\left(\frac{\Psi_g - V - V_{th}}{V_{thermal}}\right)$ and W is

The Lambert-W function which is defined as the inverse function of $y=xe^x$ [12]. Figure 2 represents the relation between the surface potential and gate voltage with quasi-Fermi potential V=0. The model is found to be in good agreement with the TCAD simulation results.

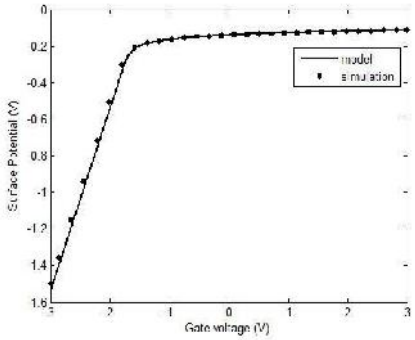


Fig. 2 Surface potential variation with gate voltage for DG JL MOSFET for quasi-Fermi potential V=0.

- **DG MOSFET**

Figure 3 shows the cross-section of a symmetric DG MOSFET. Both the gates have same gate voltage having same work function.

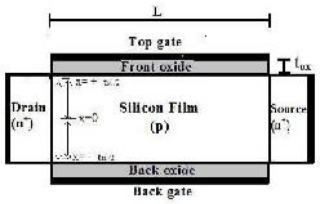


Fig. 3 Cross-section of DG MOSFET

Considering only the mobile charge carriers, the Poisson's equation in the channel region is given by:

$$\frac{d^2\Psi_{dg}}{dx^2} = \frac{qn_i}{\varepsilon_{si}}\left(\exp\left(\frac{\Psi_{dg}}{V_{thermal}}\right)\right) \quad \ldots (15)$$

where $\Psi_{dg}(x)$ is the electrostatic potential for the double gate (DG) MOSFET, n_i is the intrinsic carrier concentration [13] and other parameters being same as that in case of DG JL MOSFET. Here the device considered is an nMOSFET with hole concentration negligible to that of the electron concentration and the silicon film is considered to be lightly doped or undoped.

Integrating (15) once with boundary condition $\left.\frac{d\Psi_{dg}}{dx}\right|_{x=0} = 0$ we obtain:-

$$\frac{d\Psi_{dg}}{dx} = \sqrt{\frac{2qn_i KT}{\varepsilon_{si}}\left[\exp\left(\frac{\Psi_{dg}}{V_{thermal}}\right) - \exp\left(\frac{\Psi_{dg0}}{V_{thermal}}\right)\right]} \quad \ldots (16)$$

Where Ψ_{dg0} is the potential at centre of the silicon film at x=0. Again integrating once the potential being the function of x is obtained as:

$$\ln\left[\cos\left(\frac{x}{2V_{thermal}}\sqrt{\frac{2n_i KT}{\varepsilon_{si}}\left(\exp\left(\frac{\Psi_{dg0}}{V_{thermal}}\right)\right)}\right)\right] = -\frac{(\Psi_{dg} - \Psi_{dg0})}{2V_{thermal}} \quad \ldots (17)$$

Thus, the surface potential $\left(\Psi_{dgs} = \Psi_{dg}\Big|_{x=\pm\frac{t_{si}}{2}}\right)$ is obtained as:

$$\Psi_{dgs} = -2V_{thermal}\ln\left[\cos\left\{\frac{n_i q}{2\varepsilon_{si}V_{thermal}}\left(\frac{t_{si}}{2}\right)\right\}\right] \quad \ldots (18)$$

The relation between the surface potential and gate voltage is expressed by using Gauss's law as:

$$\frac{\varepsilon_{ox}}{t_{ox}}\left(\Psi_g - \Delta\Phi_i - \Psi_{dgs}\right) = \pm\varepsilon_{si}\frac{d\Psi_{dg}}{dx} \quad \ldots (19)$$

Where $\Delta\phi_i$ is the work function difference between gate and intrinsic silicon.

By using (16) the relation between surface potential and gate voltage is given by:-

$$\Psi_g = \Psi_{dgs} + \Delta\phi_i + \frac{\sqrt{2qn_i K T \varepsilon_{si}}\exp\left(\frac{\Psi_{dgs}}{V_{thermal}}\right)}{C_{ox}} \quad \ldots (20)$$

Figure 4 shows the plot of surface potential versus gate voltage for DG MOSFET. The model is found to be in good agreement with the TCAD simulation results.

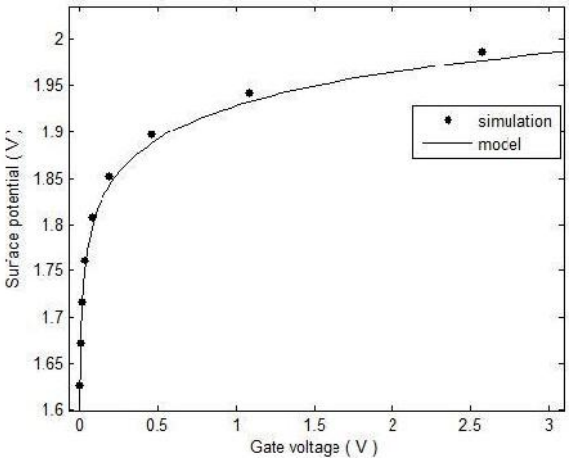


Fig. 4 Surface potential variation with gate voltage for undoped symmetrical DG MOSFET

The threshold voltage for a symmetrical DG MOSFET is given by [14]:

$$V_{th} = \left[\frac{E_g}{2q} + V_{bi} + \frac{\phi_{gfs}(1+r) - \left(\frac{b}{C_{ox}} - r\frac{b}{2C_{si}}\right)}{1+r} - \frac{3t_{si}t_{ox}V_{DS}}{L^2} - \frac{9t_{si}t_{ox}\left(\frac{E_g}{2q}\right)}{L^2}\right] \quad \ldots (21)$$

Where E_g is the energy band gap for silicon, V_{bi} is the built in potential ($\frac{KT}{q}\left(\frac{N_A}{n_i}\right)$) doping concentration, ϕ_{gfs} is the work function Difference between the gate electrode and the body region, $Q_b = -qN_At_{si}$ is the depletion charge density, factor.

C_{ox} is the oxide capacitance, $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$ is silicon film

capacitance, $r = \frac{3t_{ox}}{3t_{ox} + t_{si}}$ is the gate to gate coupling

Drain Current Model 3.1 DG JL MOSFET

Using the gradual channel approximation, the drain current equation can be expressed by Pao-Sah integral as:

$$I_{drain} = -\frac{W_{jl}}{L}\int_0^{V_D} Q_{mobile}\, dV \qquad \ldots (22)$$

where $Q_{mobile} = Q_0 - Q_D$ is the mobile charge density, $Q_D = qN_{si}t_{si}$ being the fixed charge density, μ is the carrier mobility which is constant along the channel, W_{jl} is the width of the DG JL MOSFET and L being the channel length. V_D is the drain voltage with the source voltage assumed to be 0.

Replacing Q_0 from (5) equation (22) is obtained as:

$$I_{drain} = \frac{W_{jl}}{L}\sqrt{2}\,\mu_n C_{ox}\int_0^{V_D}\left[(\Psi_{js} - \Psi_{s0} - \Psi_{a0}) + n_a\right]dV \qquad \ldots (23)$$

A compact analytical model for the subthreshold drain current model is developed using the surface potential equation in (14).For subthreshold region, $\Psi_{js} < \Psi_{s2}$, the channel of DG JL MOSFET is fully depleted. Differentiating (14) with respect to Ψ_{jls} leads to:

$$\frac{dV}{d\Psi_{jls}} = \left[\frac{1+W(A)}{W(A)}\right] \qquad \ldots (24)$$

Solving (23) we obtain:-

$$I_{drain} = \frac{W_{jl}}{L} v_{therml} 2C_{ox}\int_0^{V_D} W[A]dV \qquad \ldots (25)$$

Using (24) in (25) we get the subthreshold drain current as:

$$I_{drain} = \frac{W_{jl}}{L} v_{therml} 2C_{ox}\int_{\Psi_{jls}(0)}^{\Psi_{jls}(L)} 1 + W[A]d\Psi \qquad \ldots (26)$$

where $\Psi_{jls(0)}$ and $\Psi_{jls(L)}$ being the surface potential at x=0 and L respectively.

Putting the limits, finally the subthreshold drain current of DG JL MOSFET is obtained as:

$$I_{drain} = \frac{W_{jl}}{L}(v_{thermal})^2 (1+s)(s-d) \qquad \ldots (27)$$

where $s = \left[\frac{N_{si}qt_{si}}{4v_{thermal}C_{ox}}\right]\left[\frac{\Psi_g - V_{th}}{v_{thermal}}\right]$ and

$$d = W\left[\frac{N_{si}qt_{si}}{4v_{thermal}C_{ox}}\exp\left(\frac{\Psi_g - V_{th} - V_D}{v_{thermal}}\right)\right]$$

with device dimension scaling, the subthreshold drain current is affected by the short channel effects such as DIBL (Drain Induced Barrier Lowering) and channel length modulation. Some parameters have been incorporated in the drain current model to account for these effects.

A drain voltage dependent parameter $\sim s_a$ accounting for DIBL is being included in the exponential term of the current model which was previously only gate voltage dependent parameter [15]. The value of as proposed by Meindl and Swanson [16] for bulk MOSFET is being modified for the case of double gate structure by adding an empirical parameter H, thereby modifying the value of as:

$$\sim = \frac{£_{si} H}{C_{OX} L} \quad \ldots (28)$$

The channel length modulation parameter [17] is represented as:

$$CLM = 1 + \left(\frac{a}{L}\right) - \frac{a}{L}\left(\frac{V_{def}}{V_{gef} - V_{th}}\right) \quad \ldots (29)$$

where is the empirical fitting parameter and

$$a = \sqrt{\frac{£_{si} t_{si}}{2C_{ox}}\left(1 + \frac{t_{si} C_{ox}}{4£_{si}} - \frac{t_{si} C_{ox}}{16£_{si}}\right)}$$ is the natural length [18].

Thus, the modified subthreshold drain current model for DG JL MOSFET is modeled as:

$$I_{drain} = «\frac{W_{jl}}{L}(v_{thermal})^2 (1 + s_1)(s_1 - d_1)(CLM) \quad \ldots (30)$$

where $s_1 = w\left[\frac{N_{si} qt_{si}}{4v_{thermal} C_{ox}} \exp\left(\frac{\sim V_D + \Psi_g - V_{th}}{v_{thermal}}\right)\right]$ and

$$d_1 = w\left[\frac{N_{si} qt_{si}}{4v_{thermal} C_{ox}} \exp\left(\frac{\sim V_D + \Psi_g - V_{th} - V_D}{v_{thermal}}\right)\right]$$

- **DG MOSFET**

The subthreshold region drain current model for DG MOSFET is given by the BSIM drain current model Introducing the DIBL and channel length modulation parameters to the drain current model, the final subthreshold region drain current model for DG MOSFET is given by:-

$$I_{drain\_dg} = \left[\frac{2W}{«C_{ox}\frac{dg}{L}(v_{thermal})^2}\left(1 - \exp\left(\frac{V_D}{v_{thermal}}\right)\right)\right]\left[\exp\left(\frac{-}{v_{thermal}}\right)\right]CLM \quad \ldots (31)$$

where $^{-} = \frac{\Psi g - Vth}{\text{swing } n} + \sim s_a, v$

is the subthreshold coefficient [18], W_{dg} is width of the device and other parameters being same as that in case of DG JL MOSFET.

Model Validation and Discussions

The results of the proposed model are being validated with the TCAD simulation tool Cogenda. A classical drift diffusion approach is being used for the simulation process and also Fermi-Dirac carrier statistics are incorporated throughout the process. The transfer characteristics of the proposed device is obtained for channel length L = 45 nm and width as W=50 nm. The effective mobility for simplicity is considered to be 500 cm^2/Vs with the assumption that the carrier mobility is constant throughout the channel and the velocity saturation effect is neglected. The gate work function is considered to be 4.74eV. An n-type uniform channel doping for the DG JL MOSFET is considered as $N_{si} = 10^{19}$ cm^{-3} and other device parameters such as oxide thickness and silicon film thickness is considered as t_{ox} =2nm and t_{si} =10nm respectively. These device parameters are considered throughout the simulation process for both DG JL MOSFET and DG MOSFET device. For DG MOSFET the doping concentration in both n and p region is considered as $N_A = N_{si} = 10^{19} cm^{-3}$.

Figure 5(a) and 5(b) represents the transfer characteristics of the DG JL MOSFET in the subthreshold region for VD=0.1V and VS=0V. The fitting parameter values considered for the drain current model are H=0.4 and =1 where the value of can be any value from 0.6 to 1.2. The figures represent the subhreshold region drain current in both logarithmic and linear scale respectively. From both the figures it is clearly observable that the proposed model and the simulation results are in good agreement with each other for the subthreshod region (VG < Vth) and deviates after that. The same analysis is being done in Figure 6(a) and 6(b) for DG MOSFET in logarithmic and linear scale respectively and both the model and simulation results are found to be in good agreement for subthreshold region.

Figure 7(a) and 7(b) compares the transfer characteristics of the proposed model for the same defined device parameters in both logarithmic and linear scale with that of a previous study [8] in which the subthreshold region drain current for DG JL MOSFET is given by:-

$$I_{drain} = \frac{W}{L} \mu_{jl} V_{thermal} \sqrt{\frac{qN_{si}\varepsilon_{si}}{2\varepsilon_{si}}} e^{X}\left(1 - e^{-Y}\right) \quad \ldots (32)$$

$$\text{where } X = \left(\frac{\Psi_{g} - V_{th}}{V_{thermal}}\right) \text{ and } Y = \left(-\frac{V_{D}}{V_{thermal}}\right)$$

From the figure it is observed that the present current model using Lambert-W function is more close to the simulation results than that of the previous model.

Parameters such as DIBL and channel length modulation were introduced in the proposed drain current model to better the device characteristics curve at higher drain voltage. Figure 8(a) and 8(b) show the logarithmic transfer characteristics curve for both DG JL MOSFET and DG MOSFET respectively at V_D = 1V and it is observed that the model is in good agreement with the simulation result at higher drain voltage.

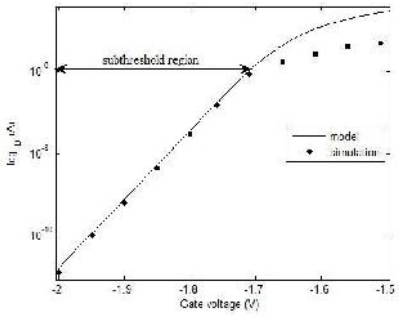


Fig. 5(a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the proposed model compared with simulation (symbols) results.

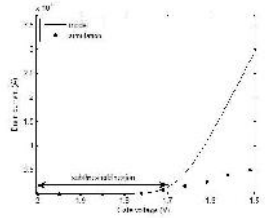


Fig. 5(b) Transfer characteristics for symmetrical DG JL MOSFET in linear scale for the proposed model compared with simulation (symbols) results.

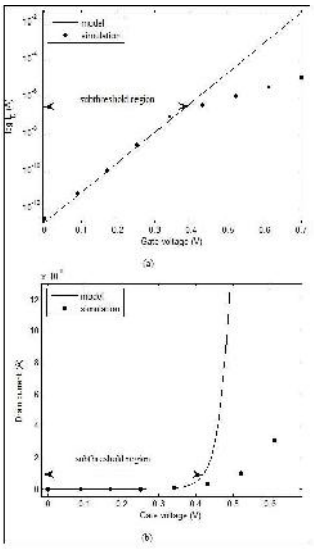


Fig. 6 Transfer characteristics for symmetrical DG MOSFET in (a) logarithmic and (b) linear scale for the proposed model compared with simulation (symbols) results.

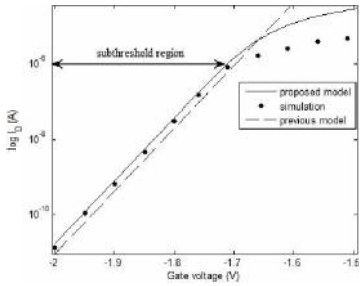


Fig. 7(a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the proposed model and previous research model compared with simulation (symbol) results.

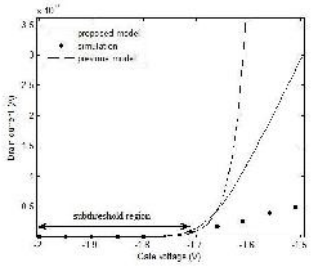


Fig. 7(b) Transfer characteristics for symmetrical DG JL MOSFET in linear scale for the proposed model and previous research model compared with simulation (symbol) results.

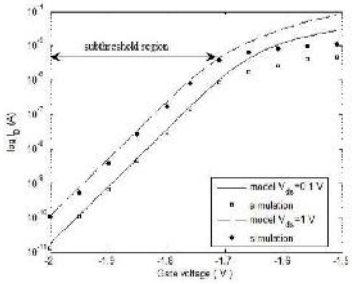


Fig. 8(a) Transfer characteristics for symmetrical DG JL MOSFET in logarithmic scale for the proposed model at V_D=1V and V_D=0.1V.

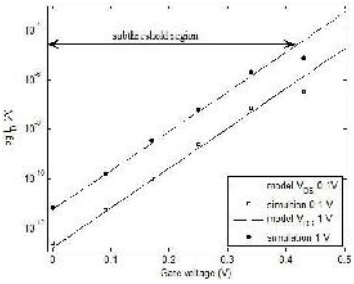
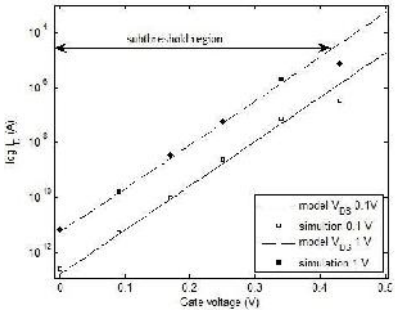


Fig. 8(b) Transfer characteristics for symmetrical DG MOSFET in logarithmic scale for the proposed model at V_D=1V and V_D=0.1V.



In DG JL MOSFET the threshold voltage shift is larger due to the presence of heavy doping in the channel region. In order to study this effect the change in threshold voltage is studied by varying the oxide thickness from 1.5nm to 3.5nm in Figure 9. The threshold voltage change with varying oxide thickness for DG MOSFE is also calculated and compared with that of DG JL MOSFET. In case of DG MOSFET with increasing oxide thickness threshold voltage increases and for DG JL MOSFET with increasing oxide thickness we observe that the negative gate voltage increases that are more number of majority charge carriers are required to turn the device into conduction.

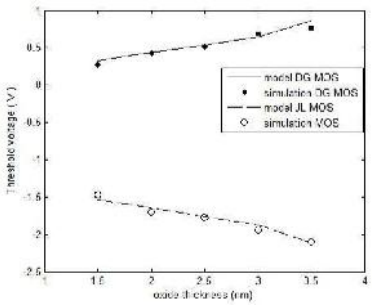


Fig. 9 Threshold voltage comparison between DG JL MOSFET and DG MOSFET for oxide thickness variation for the proposed model and simulation results

Conclusions

With the scaling of device dimensions, a need to suppress the short channel effects was felt and DG JL MOSFET is one of the promising future candidates in the field of device technology. In this paper n-type DG JL MOSFET was explored to study its behavior. An analytical compact drain current model in the subthreshold region was developed and the model was validated with the simulation results and was found to be in good agreement. The proposed model characteristics was compared to the DG MOSFET characteristics curve and was found that the proposed model follows all the characteristics of a short channel device.

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