International Journal of Education, Modern Management, Applied Science & Social Science (IJEMMASSS)
ISSN : 2581-9925, Impact Factor: 5.143, Volume 02, No. 03, July - September, 2020, pp.193-203

DRAIN CURRENT AND THRESHOLD VOLTAGE MODELING FORLIGHTLY DOPED SYMMETRICAL DOUBLE-GATE MOSFETs

Dr. Satish Chand Singhal*

ABSTRACT

A two dimensional model for the potential distribution in the silicon film is derived for the symmetrical double gate MOSFET in weak inversion. This 2D potential distribution model is used to analytically derive an expression for the sub threshold slope and threshold voltage. A drain current model for lightly doped symmetrical DG MOSFET is then presented by considering weak and strong inversion regions including short channel effects, series source to drain resistance and channel length modulation parameters. These derived models are compared with the simulation results of SILVACO (Atlas) tool for different channel lengths and silicon film thicknesses. Lastly the effect of the fixed oxide charge on the drain current model has been studied through simulation. It is observed that the obtained analytical models of symmetrical double gate MOSFET is in good agreement with the simulated results for channel length to silicon film thickness ratio greater than or equal to 2.

Keywords: *DG-MOSFET, Short Channel Effect (SCE), Threshold Voltage, SILVACO.*

Introduction

Double gate metal-oxide-semiconductor field-effect-transistor (DG-MOSFETs) has enormously succeeded in overcoming the drawbacks present in single-gate MOSFET architectures with channel length of 65nm and below. Double gate MOSFET offers vast variety of advantages such as high drive current, gate leakage reduction, low leakage currents through PN junctions and reduced short channel effects [1]-[4]. The lightly doped silicon film in ultrathin DG-MOSFETs provide an added advantage of elimination of mobility degradation [5] and deviation of device characteristics with non-uniform dopant atoms present in the silicon film [6].

Analytical modeling of the current-voltage relationship of symmetrical double gate MOSFET at nanometer domain is highly required as it is becoming a favorable choice for designing nanometer range VLSI circuits. Many analytical models for the drain current of long channel DG MOSFET have been proposed [7]-[12]. Appropriate analytical drain current model considering major effects for small channel lengths below 45nm is still a matter under research. In this paper, the sub threshold drain current equation valid for the entire range of drain voltages is modeled including channel length modulation, DIBL and other SCEs embedded within the threshold voltage. Further, a total drain current expression is obtained involving the modeled sub threshold drain current and strong inversion drain current [26] equations. The fixed oxide charge effect over the drain current is also studied. The model is verified by comparing the results obtained from SILVACO (Atlas) TCAD tool. The important parameters required for the drain current equation such as channel potential, sub threshold coefficient, threshold voltage and threshold voltage roll-off are also derived and verified.

Potential Distribution

In order to obtain the physical behavior of symmetrical DG MOSFET at nanometer domain the potential distribution across the thin silicon film under different drain and gate bias conditions must be explicitly studied. Presence of two gates and thin silicon film causes the potential distribution in DG MOSFET to be different than single gate MOSFETs and the maximum potential do not occur at the surface but at some depth of the silicon film [23]. In this paper depletion approximation is used for solving weak inversion Poisson's equation to analytically determine the potential distribution in silicon film.

---

* Associate Professor, Department of Physics, Sri SantSuderdas Government Girls PG College, Dausa, Rajasthan, India.

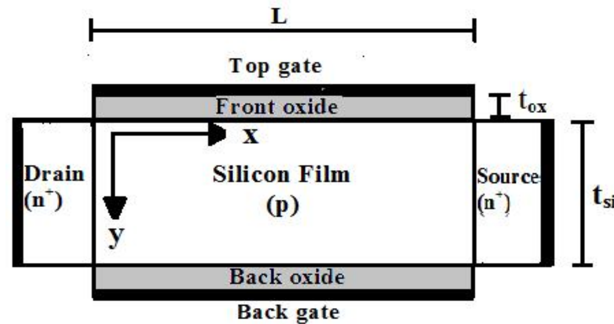

Fig.1: Schematic diagram of symmetric n-channel Double Gate MOSFET with structural definition and coordinate system

The Poisson's equation in the form of electric field variation along the three dimensions can be written as:-

$$\frac{\partial \vec{E}_x}{\partial x} + \frac{\partial \vec{E}_y}{\partial y} + \frac{\partial \vec{E}_z}{\partial z} = \frac{qNa}{\epsilon_{Si}} \quad (1)$$

where, $\vec{E}_x = \frac{\partial \phi(x,y,z)}{\partial x}$, $\vec{E}_y = \frac{\partial \phi(x,y,z)}{\partial y}$, $\vec{E}_z = \frac{\partial \phi(x,y,z)}{\partial z}$ are the electric field component in x, y and z direction respectively and $\phi(x, y, z)$ is the channel potential. This equation predicts that the sum of electric field variation at any point in the silicon film is always a constant whose value is given through the ratio of depletion region charge and permittivity of the material. Thus, for equilibrium it is necessary that if any one or two component of the electric field changes then the other should also vary to keep their sum a constant. The drain electric field influence on the channel is represented by $\vec{E}_x$ and its large value is responsible for causing various SCEs in the device. This drain electric field can be reduced by increasing channel length, using multi-gate architectures and reducing silicon film thickness and/or channel width.

The electric field variation along the z direction in large width DG MOSFET scan be considered as zero which reduces (1) to

$$\frac{\partial \vec{E}_x}{\partial x} + \frac{\partial \vec{E}_y}{\partial y} = \frac{qNa}{\epsilon_{Si}} \quad (2)$$

For strong inversion region (2) is not valid as then the channel potential along x is modulated by inversion charge[13]-[14]. To solve (2), the potential distribution along the silicon film thickness is taken as a cubic function of xas proposed by Toyabe and Asai [15].

$$\phi(x, y) = a_0(y) + a_1(y)x + a_2(y)x^2 + a_3(y)x^3 \quad (3)$$

where, coefficients a_0, a_1, a_2 and a_3 are the function of y dimension only. In symmetrical DG-MOSFET due to structural symmetry the front and back oxide-silicon interface have same potential distribution along the channel which can be defined as

$$\phi(x, 0) = \phi(x, t_{si}) = \phi_1(x) \quad (4)$$

The boundary conditions are obtained by applying gauss law in vertical direction at the gate oxide transverse electric field $\vec{E}_y$ on both front and back gates.

$$\vec{E}_y(\text{at } y = 0) = \frac{Q_0}{\epsilon_{Si}} \quad (5)$$

$$\vec{E}_y(\text{at } y = t_{si}) = \frac{Q_{t_{si}}}{\epsilon_{Si}} \quad (6)$$

where, $Q_0 = C_{ox}V_f$ and $Q_{t_{si}} = C_{ox}V_b$ are the net charges atthe front and back oxide-silicon interface respectively with gate oxide capacitance per unit area given as $C_{ox} = \epsilon_{ox}/t_{ox}$ in terms of permittivity of gate oxide (ϵ_{ox}) and oxide thickness (t_{ox}). $V_f = \phi_1(x) - V_g'$ and $V_b = V_g' - \phi_1(x)$ represents voltage difference along the oxide thickness at both front and back gates responsible for capacitive action. The virtual gate voltage (V_g') appearing at the front and back gate is always smaller than the actual applied gate voltage (V_g) as some amount of gate voltage is utilized in cancelling out the effect of contact potentials and potential developed due to fixed

oxide charges which is collectively known as flatband voltage (V_{FB}). The flatband voltage assuming fixed oxide charges to be zero is given by the work function difference between the metal and semiconductor (W_{ms}), whose value is $-(KT/q)\ln\frac{Na}{ni}$ for mid-gap metal gates

To obtain the coefficient values of the cubic potential distribution(4)-(6) are used in (3)

$$a_0 = \phi_1(x) \qquad (7)$$

$$a_1 = \frac{C_{ox}V_f}{\epsilon_{Si}} \qquad (8)$$

$$a_2 = -\frac{a_1}{t_{si}} = \frac{C_{ox}V_b}{\epsilon_{Si}} \qquad (9)$$

$$a_3 = 0 \qquad (10)$$

Solving (3) and (2) using (7)-(10), a differential equation in terms of surface potential is obtained as

$$\frac{\partial^2\phi_1(x)}{\partial x^2} - \beta_0\phi_1(x) = \beta_1 \qquad (11)$$

where,

$$\beta_0 = \frac{2C_{ox}}{\epsilon_{Si}t_{si} + C_{ox}t_{si}y - C_{ox}y^2} \text{ and } \beta_1 = \frac{qN_a t_{si} - 2C_{ox}V_g'}{\epsilon_{Si}t_{si} + C_{ox}t_{si}y - C_{ox}y^2}$$

Next, solving (11) using boundary conditions $\phi_1(x) = \phi_{bi}$ at x=0 and $\phi_1(x) = \phi_{bi} + V_d$ at x=L, where $\phi_{bi} = V_T \ln N_a N_d / n_i^2$ is the built in potential, $V_T = kT/q$ is the thermal voltage, N_a is the acceptor concentration, N_d is the donor concentration, n_i is the intrinsic carrier concentration and V_d is the applied drain voltage. The expression for surface potential thus obtained is

$$\phi_1(x) = c_1 e^{x/\lambda_1} + c_2 e^{-x/\lambda_1} + A_1 \qquad (12)$$

where, c_1 and c_2 are the coefficients and A_1 is a constant given as

$$c_1 = \frac{\phi_{bi}(1 - e^{-L/\lambda_1}) + V_d + A_1(e^{-L/\lambda_1} - 1)}{(e^{L/\lambda_1} - e^{-L/\lambda_1})}$$

$$c_2 = \frac{\phi_{bi}(1 - e^{L/\lambda_1}) + V_d + A_1(e^{L/\lambda_1} - 1)}{(e^{-L/\lambda_1} - e^{L/\lambda_1})}$$

$$A_1 = \frac{-\beta_1}{\beta_0} = V_g' - \frac{qN_a t_{si}}{2C_{ox}}$$

where, λ is the natural length and λ_1 is its value at y=0 and t_{si} [16].Natural length is defined as the parameter which indicates the drain field influence on the channel characterizing the SCE. It mainly depends on the geometrical dimensions and its value should be as small as possible. The natural length can be given as shown below

$$\lambda = \frac{1}{\sqrt{\beta_0}} = \sqrt{\frac{\epsilon_{Si}t_{si} + C_{ox}t_{si}y - C_{ox}y^2}{2C_{ox}}} \qquad (13)$$

$$\lambda_1 = \frac{1}{\sqrt{\beta_0(\text{at } y=0)}} = \sqrt{\frac{\epsilon_{Si}t_{si}}{2C_{ox}}} \qquad (14)$$

In DG MOSFETs the surface potential is less than the potential at the effective conductive path taken at $y = t_{si}/4$ [1].Thus, itis necessary to determine the potential as the function of channel depth by defining the potential in terms of surface potential using (3).

$$\phi(x,y) = \alpha_1\phi_1(x) - \alpha_2 V_g' \qquad (15)$$

where, $\alpha_1 = 1 + \frac{C_{ox}y}{\epsilon_{Si}} - \frac{C_{ox}y^2}{\epsilon_{Si}t_{si}}$ and $\alpha_2 = \frac{C_{ox}y}{\epsilon_{Si}} - \frac{C_{ox}y^2}{\epsilon_{Si}t_{si}}$

Using (15) and (11) a differential equation for potential distribution can be obtained as

$$\frac{\partial^2\phi(x,y)}{\partial x^2} - \beta_0'\phi(x,y) = \beta_1' \qquad (16)$$

where, $\beta_0' = \beta_0$

$$\beta_1' = \frac{2C_{ox}V_g'(C'-1) + qN_a t_{si}}{\epsilon_{Si}\, t_{si}}$$

$$C' = \frac{C_{ox}t_{si}y - C_{ox}y^2}{\epsilon_{Si}\, t_{si} + C_{ox}t_{si}y - C_{ox}y^2}$$

The solution (16) using boundary conditions $\phi(x,y) = \phi_{bi}$ at x=0 and $\phi(x,y) = \phi_{bi} + V_d$ at x=L is expressed as

$$\phi(x,y) = c_1' e^{x/\lambda} + c_2' e^{-x/\lambda} + A_2 \quad (17)$$

where,

$$c_1' = \frac{\phi_{bi}\left(1 - e^{-L/\lambda}\right) + V_d + A_2\left(e^{-L/\lambda} - 1\right)}{\left(e^{L/\lambda} - e^{-L/\lambda}\right)}$$

$$c_2' = \frac{\phi_{bi}\left(1 - e^{L/\lambda}\right) + V_d + A_2\left(e^{L/\lambda} - 1\right)}{\left(e^{-L/\lambda} - e^{L/\lambda}\right)}$$

$$A_2 = \frac{-\beta_1'}{\beta_0'} = V_g' - \frac{qN_a(\epsilon_{Si}\, t_{si} + C_{ox}t_{si}y - C_{ox}y^2)}{2\, C_{ox}\, \epsilon_{Si}}$$

Substituting the values of yas 0 andt_{si}, (17) reduces to (13).

Minimum Potential

The channel position x_{min} at which the channel potential reaches its minimum value (ϕ_{min}) can be determined by considering potential minima along x direction [16].

$$\frac{\partial\phi(x,y)}{\partial x}(\text{at } x_{min}) = 0$$

$$x_{min} = \frac{L}{2} - \frac{\lambda}{2}\ln\left[\frac{(\phi_{bi} - A_2)(e^{L/\lambda} - 1) + V_d e^{L/\lambda}}{(\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d}\right] \quad (18)$$

The position at which minimum channel potential occurs depend on the applied drain voltage and it can be seen that for zero drain voltage the minimum channel potential is at the middle of the channel length while it moves towards the source end as the drain voltage increases. The value of ϕ_{min} evaluated using (17) and (18) is

$$\phi_{min} = c_1' e^{x_{min}/\lambda} + c_2' e^{-x_{min}/\lambda} + A_2 \quad (19)$$

Sub Threshold Slope

The sub threshold slope (SS) is determined through the C-V characteristic as$SS = (\partial V_g / \partial \log I_D)$ but aanalytically the sub threshold slope expression can be obtained based on the assumption that SS basically depends on the carrier concentration n_{min} at minimum channel potentialϕ_{min} located at a depth y in the silicon film[18]-[19]. The carrier concentration n_{min} is given by$n_{min} = (n_i^2/N_a)\, e^{\phi_{min}/V_t}$.

$$SS = \frac{\partial V_g}{\partial \log I_D} \approx \ln 10 \frac{\partial V_g}{\partial \ln n_{min}} = \frac{V_T \ln 10}{\partial\phi_{min}/\partial V_g} \quad (21)$$

where,

$$\frac{\partial\phi_{min}}{\partial V_g} = 1 + \frac{1}{(e^{2L/\lambda} - 1)}\left[\left(e^{3L/2\lambda} - e^{L/2\lambda}\right)\left((\phi_{bi} - A_2)X_1 - Ps\right) + X_2\right] \quad (22)$$

$$Ps = \left(x_s^{-1/2} + x_s^{1/2}\right)$$

$$X_1 = \frac{1}{2}\left[\frac{V_d\left(e^{2L/\lambda} - 1\right)}{\left((\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d\right)^2}\right]\left(x_s^{-1/2} - x_s^{-3/2}\right)$$

$$x_s = \frac{(\phi_{bi} - A_2)\left(e^{L/\lambda} - 1\right) + V_d e^{L/\lambda}}{(\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d}$$

$$X_2 = -\frac{1}{2}V_d\left[\frac{V_d\left(e^{2L/\lambda}-1\right)}{\left((\phi_{bi}-A_2)(e^{L/\lambda}-1)-V_d\right)^2}\right]\left(e^{3L/2\lambda}x_s^{-3/2}-e^{L/2\lambda}x_s^{-1/2}\right)$$

The sub threshold swing coefficient also known as the body effect coefficient is given in terms of sub threshold slopeas

$$n = \frac{SS}{V_T \ln 10} = \frac{1}{\partial\phi_{min}/\partial V_g} \quad (23)$$

Figure 2 shows that the calculated values from the analytical sub threshold slope expression obtained in (21) is in good agreement with the simulated result for all values of channel length that is taken into consideration. The device dimensions taken are, $W_{ms} = 4.74eV$, $t_{si} = 10nm$, $t_{ox} = 2nm$, $N_a = 10^{15}cm^{-3}$, $N_d = 10^{20}cm^{-3}$, W=50nm, $V_d = 1V$at an effective conducting path of$y = t_{si}/4$.

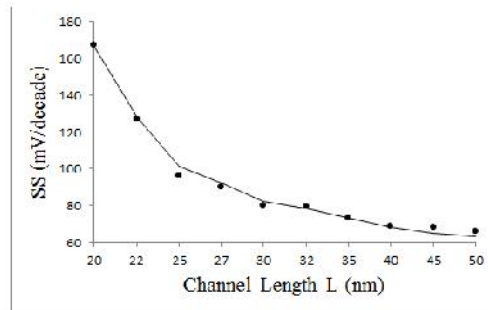

Fig.2. Comparison between the simulated (symbol) and analytical modeled (solid lines) subthreshold slope versus channel length.

Threshold Voltage

For ultra-thin DG-MOSFET with very small silicon film doping $N_a \leq 10^{16}cm^{-3}$,the threshold voltage definition may be given as the gate voltage where minimum inversion sheet charge density (Q_{inv}), required for current conduction reaches to its threshold value,Q_{th} [21].

At minimum channel potential the inversion sheet charge density can be obtained by integrating their spatial charge density for the entire thickness of the silicon film.

$$Q_{inv} = \int_0^{t_{si}} n_i e^{\phi_{min}/V_T} dy = t_{si} n_i e^{\phi_{min}/V_T} \quad (24)$$

At gate voltage equal to the threshold voltage V_{th} the value of inversion charge is $Q_{inv} = Q_{th}$. Upon evaluating (24) the expression for V_{th} obtained is

$$V_{th} = V_{FB} + \frac{qN_a(\epsilon_{Si} + 3C_{ox}t_{si}/16)}{2\,C_{ox}C_{Si}} + B_1\kappa - B_2(\phi_{bi}-\kappa)^{1/2}$$
$$(\phi_{bi} + V_d - \kappa)^{1/2} - B_3(2\phi_{bi} + V_d) \quad (25)$$

Where,$\kappa = V_T \ln\frac{Q_{th}}{n_i t_{si}}$

$$B_1 = \frac{(e^{2L/\lambda}-1)^2}{(e^{L/\lambda}-1)}$$

$$B_2 = \frac{2\left(e^{5L/2\lambda}-e^{L/2\lambda}\right)}{(e^{L/\lambda}-1)^3}$$

$$B_3 = \frac{2e^{L/2\lambda} - 2e^{L/\lambda}(1-2e^{L/\lambda})}{(e^{L/\lambda}-1)^4}$$

where, $C_{si}$is the silicon film capacitance per unit area given as the ratio of permittivity of silicon (ϵ_{Si}) and silicon film thickness (t_{si}).In long channel devices since the value of $\phi(x,y) = A_2$thus, the threshold voltage for long channel DG MOSFET is given as

$$V_{th} = V_{FB} + \frac{qN_a(\epsilon_{si}+3C_{ox}t_{si}/16)}{2\,C_{ox}C_{si}} + \kappa \quad (26)$$

Expressions in (25) and (26) though similar to the work done in [21], have an extra term to get more accurate value of threshold voltage.

The threshold voltage roll-off showing the drop in threshold voltage of a device with reduction in its channel length can be determined by taking the difference of short channel threshold voltage andlong channel threshold voltageat a particular drain voltage. The analytical expression of threshold voltage thus obtained is

$$\delta V_{th} = (B_1 - 1)\kappa - B_2(\phi_{bi} - \kappa)^{1/2}(\phi_{bi} + V_d - \kappa)^{1/2} - B_3(2\phi_{bi} + V_d) \quad (27)$$

The proposed analytical threshold voltage model given by (25) is compared with the simulated values of V_{th}against L for t_{si}= 5, 10 and 15nm respectively in Fig.3. It can be easily seen that the analytical threshold voltage values agree well with simulated values over complete range of investigated channel lengths when the ratio of channel length to channel thickness is $L/t_{si} \geq 2$, while it deviates for$L/t_{si} < 2$.The value of Q_{th} has been evaluated from the expression given as

$$Q_{th} = 2 \times 10^{15} + \frac{1.9\times10^{12}}{L(m)}\,m^{-2} \quad (28)$$

Which is generally obtained through a relationship that best matches the analytical expression with the simulation results.

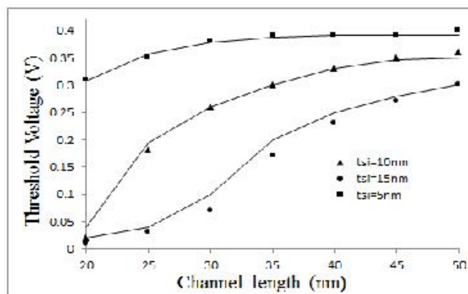

Fig.3: Threshold voltage of undoped DG MOSFET at different silicon film thickness and channel length. The symbols are simulated values while the solid lines represent the analytical values.

Drain Current

To study the behavior and evaluate the characteristics of the DG-MOSFET it is necessary to divide the transistor operation in two major regions of weak and strong inversion. The current conduction mechanism from source to drain and the factors constituting current in these two regions are different as in weak inversion the current is due to diffusionbecause of few minority carriers and depletion region generated potential distribution and in strong inversion it is thedrift current generated by the flow of inversion layer carriers under the electric field influence in the channel.

Sub Threshold Region Current ($I_{D,sub}$)

Subthreshold region also known as weak inversion region occurs at gate voltages lower than threshold voltage. The current in this region is basically due to minority carrier diffusion along the channel. The subthreshold current influenced by lower drain voltages close to 0V are modeled by BSIM drain current model [23].But at high drain voltages, DIBL and channel length modulation influence the device characteristics to a large extent. In order to account these effects additional parameters are included in the sub threshold drain current equation from[25]. Thus, an improved model is obtained for sub threshold current of symmetrical DG-MOSFET.

The channel length modulation representing the shortening of channel length at higher drain voltages due to large drain field[25] can be modeled as

$$CLM = 1 + \left(\frac{\lambda}{L}\right)^{u-\sqrt{\lambda/L}}\left(\frac{V_{def}}{V_{gef}-V_{th}}\right) \quad (29)$$

Where, u is an empirical fitting parameter having the value in the range of 0.6 to 1.2.

Drain induced barrier lowering introduced at high drain voltages is modeled by introducing a drain voltage dependent parameter ηV_d in the exponential term which was earlier only the function of gate voltage($e^{V_g - V_{th}/n}$) [26]. The DIBL parameter proposed by Meindl and Swanson [24] for bulk MOSFETs is changed for DG-MOSFET by using an empirical parameter Dandis expressed as

$$\eta = \frac{\epsilon_{si} D}{C_{ox} L} \quad (30)$$

Thus, the sub threshold current equation thus, obtained for DG MOSFET is given as

$$I_{D,sub} = \mu C_{ox} \frac{2W}{L} V_T^2 e^{\varphi/V_T}\left(1 - e^{-V_d/V_T}\right) CLM \quad (31)$$

where, $\varphi = \frac{(V_g - V_{th})}{n} + \eta V_d$, n is the sub threshold coefficient taken from (23) andV_{th} is the short channel threshold voltage (25)

Strong Inversion Current

The strong inversion drain current [25] is expressed as

$$I_{D,si} = \frac{\mu C_{si}}{1 + \frac{4\mu W C_{ox}}{L} R_{sd}(V_g - V_{th})} \frac{16W}{L} V_T^2 \left[(q_s - q_d) - \frac{C_{si}}{C_{ox}}(q_s{}^2 - q_d{}^2)\right] CLM \quad (32)$$

The R_{sd} term accounts for the series source/drain resistance, CLM gives the channel length modulation from (29) and V_{th} is the short channel threshold voltage taken from (25). The normalized sheet charge density q_i is given through lambert function as

$$q_i = \frac{C_{ox}}{2C_{si}} \text{lambertW}\left[\frac{q}{C_{ox}} \sqrt{\frac{n_i^2 \, \epsilon_{Si}}{2KTN_a}} \, e^{\frac{V_g - \delta V_{th} - V_{FB} - V}{2V_T}}\right]$$

Where, V is the electron quasi fermi potential varying from 0V at the source to $V_d$at the drain. Thus the source normalized sheet charge density (q_s) is calculated at V=0 and drain normalized sheet charge density(q_d) is obtained at V=V_d. The SCE is included by the δV_{th} parameter from (28).

To obtain a compact drain current model a suitable interpolation function is used to match the sub threshold and strong inversion modes around threshold voltage of the form as follows

$$I_D = \frac{I_{D,sub} \times I_{D,si}}{(I_{D,sub}{}^{\alpha} + I_{D,si}{}^{\alpha})^{1/\alpha}} \quad (33)$$

Equation (33) gives the drain current in the DG MOSFETat all values of gate and drain voltages.

Model Validation

The results obtained from the proposed model are validated by comparing it with the SILVACO (atlas) simulator results using the classical drift diffusion approach. The output and transfer characteristics are obtained for two different channel lengths L=32nm and 45nm.The geometrical dimensions of the device are same as taken for other simulations and for simplicity a constant mobility of $\mu = 500 \text{ cm}^2/\text{Vs}$ is used ignoring mobility degradation and velocity saturation effect. The interpolation function expression is $\alpha = 1.9 - \sqrt{1.2V_{ds}}$it is chosen such that it best fits the simulation results.

Figure 4 and 5 shows the characteristics of the symmetrical DG-MOSFET for a channel length of 32nm and 45 nm respectively with zero series source /drain resistance by keeping the source/drain length 5 nm. The output characteristic shown in Fig. 4 and 5 (a) is obtained at three different gate voltages V_g= 0.65, 0.8 and 1V. Similarly the linear and semi-logarithmic representation of the transfer characteristic shown in Fig. 4 and 5 (b) are obtained for drain voltages V_d= 0.02, 0.3 and 1V giving the model accuracy in both weak and strong inversion regions. The threshold sheet charge carrier density used to define the threshold voltage is taken as$Q_{th} = 2.8 \times 10^{15} \text{cm}^{-2}$for evaluation. Good agreement is achieved between the simulated and analytical results for both the channel lengths.

In Fig.6 the C-V characteristics of the analytical model is examined for a series resistance of $R_{sd} = 180\,\Omega$ by taking the source/drain lateral length 50nm. Fig.6(a) shows the output characteristic while Fig. 6(b) shows the linear and semi-logarithmic representation of the transfer characteristic at different gate and drain voltages to verify the results for all regions of operation of a MOSFET. The proposed model is thus validated for different channel lengths and series resistances in all regions of operation showing remarkable agreement with the simulated results.

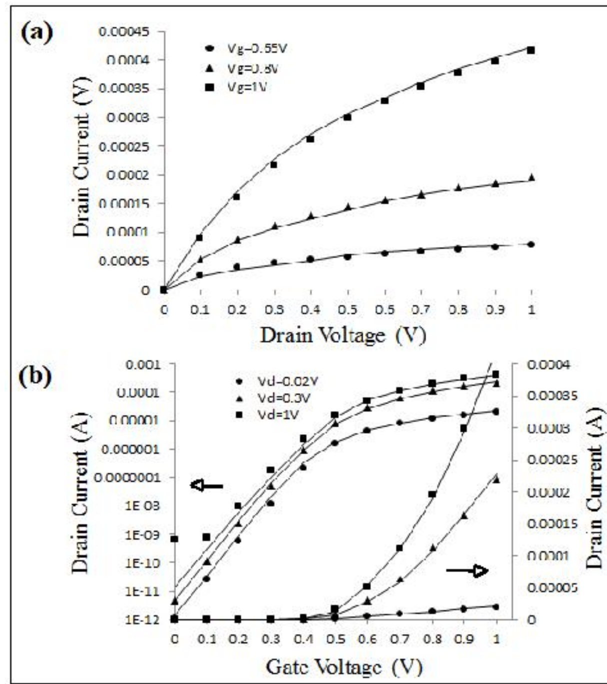

Fig.4: simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic representation in linear and semi-logarithmic form for symmetrical DG MOSFET for L=32nm, t_{si}=10nm, t_{ox}=2nm, R_{sd}=0 .

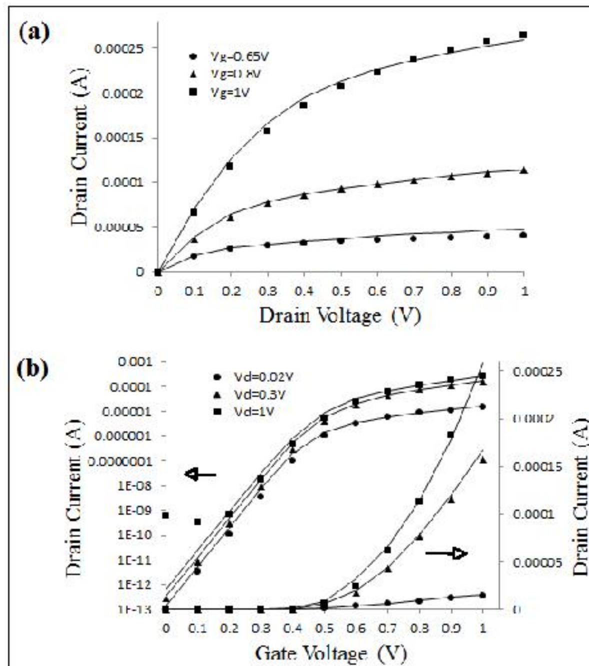

Fig.5: Simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic representation in linear and semi-logarithmic formfor symmetrical DG MOSFET for L=45nm, t_{si}=10nm, t_{ox}=2nm andR_{sd}=0 .

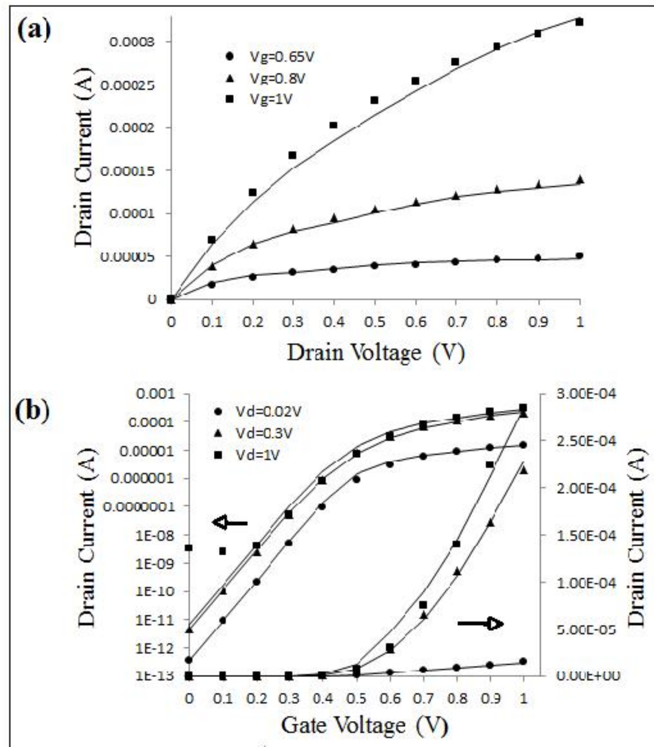

Fig.6: Simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic representation in linear and semi-logarithmic form for symmetrical DG MOSFET for L=32nm, t_{si}=10nm, t_{ox}=2nm andR_{sd}=180 .

The obtained current model is also studied by considering the effect of fixed oxide charges present in thin oxide layers. This effect is included in the flatband voltage expression as

$$V_{FB} = W_{ms} - \frac{qN_f}{C_{ox}} \quad (35)$$

Where, W_{ms} represents the work function difference between the metal and the semiconductor for the mid-gap metal gates. $N_f$is the fixed oxide charge density in cm^{-3}. Figure 7 shows the effect offixed oxide charge on the modeled and simulated drain current for different gate voltages.

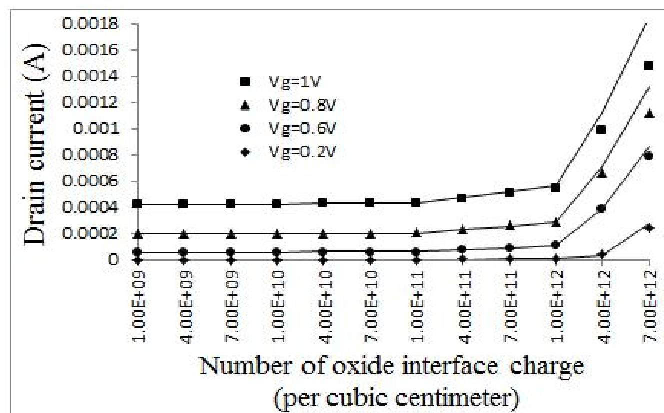

Fig. 7. Drain current variation simulated (symbol) and model (solid lines) with the oxide interface charge at different gate voltages

Conclusion

A 2D potential distribution based sub threshold slope and threshold voltage expressions have been obtained and embedded within the drain current model of symmetrical DG-MOSFET. These analytical model expressions are verified with the simulated results of SILVACO (Atlas) tool.

The sub threshold slope and threshold voltage variation considering different channel length for the device have been obtained. The output and transfer characteristics of the proposed drain current model at different channel lengths and series source to drain resistance are compared with the simulation results. Finally, the effect of fixed oxide charges have been observed and compared with simulation results. The developed drain current model is in good agreement with the simulated results and may be feasible for compact model applications for well-designed devices with $L/t_{si} \geq 2$.

References

1. S.-H. Oh, D. Monroe, and J. M. Hergenrother, “Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs,” IEEE Electron Device Lett., vol. 21, no. 9, pp. 445–447, Sep. 2000.
2. D. Jimenez, B. Iniguez, J. Sune, J.J. Saenz, “Analog performance of the nanoscale double-gatemetal-oxide-semiconductor field-effect-transistor near the ultimate scaling limits”Journal of Applied Physics., vol. 96, no. 9, pp. 5271–5276, Nov. 2004.
3. Q. Chen, E. M. Harrell, and J. D. Meindl, “A physical short channelthreshold voltage model for undoped symmetric double–gateMOSFETs,” IEEE Trans. Electron Devices, vol. 50, no. 7,pp. 1631–1637, Jul. 2003.
4. H. Abd El Hamid, J.R. Guitar, B. Iniguez, “Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double-Gate MOSFETs”IEEE Trans. Electron Devicesvol.54,pp.1402–1408, Jun 2007..
5. T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S.Tyagi, and M. Bohr, “Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors,” in VLSISymp. Tech. Dig., pp. 174-175, Jun. 2000.
6. X. Tang, V. K. De, and J. D. Meindl, “Intrinsic MOSFET parameter fluctuations due to random dopant placement,” IEEE Trans. Very LargeScale Integr. (VLSI) Syst., vol. 5, no. 4, pp. 369–376, Dec. 1997.
7. S. Malobabic, A. Ortiz-Conde, F.J. Garcia Sanchez, “Modeling the Undoped-Body Symmetric Dual-Gate MOSFET”Proc. Fifth Int. Caracas Conf. on Devices, Circuits and Systems, Dominican Republic, pp. 19–25, Nov. 2004.
8. Y. Taur, X. Liang, W. Wang, H. Lu,“A continuous, analytic drain-current model for DG MOSFETs” IEEE Electron Device Lett., vol.25, pp.107–109, Feb.2004.
9. X. Liang and Y. Taur, “A 2-D analytical solution for SCEs in DG-MOSFETs,” IEEE Trans. Electron Devices, vol. 51, no. 9, pp. 1385–1391,Sep. 2004.
10. J.-S. Park, S. Lee, Y. Jhee, H. Shin,“Charge-Based Analytical Current Model for Asymmetric Double-Gate MOSFETs”, J. Korean Phys. Soc.Vol.47, pp. S392–S396, Nov. 2005.
11. Ortiz-Conde, F.J. Garcia-Sanchez, J. Muci,“Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs”, Solid-State Electron.,Vol.49,pp. 640–647, Apr. 2005.
12. J.M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, C.C. Enz,“A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism”,Solid-State Electron,vol. 49, pp. 485–489, Mar. 2005.
13. Y.Taur,“Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs,” IEEE Trans. Electron Devices, vol. 48, no. 12, pp. 2861–2869, Dec. 2001.
14. Q. Chen and J. D. Meindl, “Nanoscale metal-oxide-semiconductor field effect transistors: Scaling limits and opportunities,” Nanotechnology, vol. 15, no. 10, pp. S549–S555, Oct. 2004.
15. T. Toyabe and S. Asai, “Analytical models of threshold voltage and breakdown voltage of short-channel MOSFET’sderived from two-dimensional analysis”,IEEE J. Solid-State Circuits, vol. SC-14, p.375, 1979.
16. R. Y. Yan, A. Ourmazd, and K. F. Lee, “Scaling the Si MOSFET: From bulk to SOI to bulk,” IEEE Trans. Electron Devices, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

17. K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs", IEEE Trans. Electron Devices, vol. 36, no. 2, pp. 399–402, Feb. 1989.

18. Y. Tosaka, K. Suzuki, and T. Sugii, "Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFETs," IEEE ElectronDevice Lett., vol. 15, no. 11, pp.466–468, Nov. 1994.

19. K. Suzuki, Y. Tosaka, and T. Sugii, "Analytical threshold voltage model for short channel double-gate SOI MOSFETs",IEEE Trans. ElectronDevices, vol. 43, no. 7, pp. 1166–1168, Jul. 1996.

20. C. T. Lee and K. K. Young, "Submicrometer near-intrinsic thin-film SOIcomplementary MOSFET's," IEEE Trans. Electron Devices, vol. 36, pp. 2537–2547, Nov. 1989.

21. Tsormpatzoglou, C.A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, G.Ghibaudo, "Threshold voltage model for short-channel undoped symmetrical double-gate MOSFETs,"IEEE Trans. Electron Devices.,vol.55, pp. 2512–2516, Sep. 2008.

22. Tsormpatzoglou, C.A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, G. Ghibaudo, "Semi-analytical modeling of short-channel effects in Si and Gesymmetrical double-gate MOSFETs,"IEEE Trans. Electron Devices.,vol.54,pp. 1943–1952, Aug. 2007.

23. B.J. Sheu, D.L. Scharfetter, P.K. Ko, M.C. Jeng, "BSIM: Berkeley short-channel IGFET model for MOS transistors," IEEE J. Solid- State Circuits.,vol.22,pp. 558–566, Aug. 1987.

24. R. M, Swanson and J. D. Meindl, "Fundamental performance limits of MOS integrated circuits," in Proc. IEEE Int. Solid-State Circuits Corf., pp. 110-111, 1975.

25. Tsormpatzoglou , D.H.Tassis , C.A. Dimitriadis , G. Ghibaudo , G. Pananakakis , N. Collaert, "Analytical modeling for the current–voltage characteristics of undoped or lightly doped symmetric double-gate MOSFETs," Microelectronic Engineering,vol.87,pp. 1764–1768, 2010.

26. Tim Grotjohn and Bernd Hoefflinger, "A parametric short channel MOS transistor model for subthreshold and strong inversion current,"IEEE Journal for solid-state circuits, vol. 19, pp. 100-112, Feb. 1984.